characterized in that the semiconductor device includes a device fabricated below the pad area (13), further comprising a second device fabricated below the device,

the device being comprised of a bypass capacitor (19),

the second device being comprised of at least one of a protection device (31) and an input/output device (12).

24. (Amended) A semiconductor device having a plurality of wiring layers in a multi-layered structure,

the semiconductor device including an inner area (11) at a surface and a pad area (13) surrounding the inner area (11) therein,

characterized in that the semiconductor device includes a device fabricated below the pad area (13), wherein said device comprises an input/output device.

25. (Amended) A semiconductor device having a plurality of wiring layers in a multi-layered structure,

the semiconductor device including an inner area (11) at a surface and a pad area (13) surrounding the inner area (11) therein,

characterized in that the semiconductor device includes a device fabricated below the pad area (13), further comprising a second device fabricated below said device,

said device comprises a bypass capacitor,

said second device comprises a protection device.

4

~~26~~. (Amended) A semiconductor device having a plurality of wiring layers in a multi-layered structure,

the semiconductor device including an inner area (11) at a surface and a pad area (13) surrounding the inner area (11) therein,

B2

characterized in that the semiconductor device includes a device fabricated below the pad area (13), further comprising a second device fabricated below said device,

said device comprises a bypass capacitor,

said second device comprises an input/output device.

5

~~30~~. (Amended) A semiconductor device having a plurality of wiring layers in a multi-layered structure,

the semiconductor device including an inner area (11) at a surface and a pad area (13) surrounding the inner area (11) therein,

characterized in that the semiconductor device includes a device fabricated below the pad

B3

area (13),

wherein said device comprises a bypass capacitor,

wherein said bypass capacitor comprises metal wire layers arranged below said pad area,

wherein each of said metal wire layers comprises a first wire and a second wire with an interlayer insulating layer being sandwiched therebetween,

said first wire being electrically connected to a voltage source,

5

said second wire being grounded, further comprising at least one of first to fourth pads in said pad area,

B3

said first pad being electrically connected to an input/output device,

said second pad being electrically connected to said first wire,

said third pad being electrically connected to said second wire,

said fourth pad being not electrically connected to said input/output device, said first wire and said second wire.